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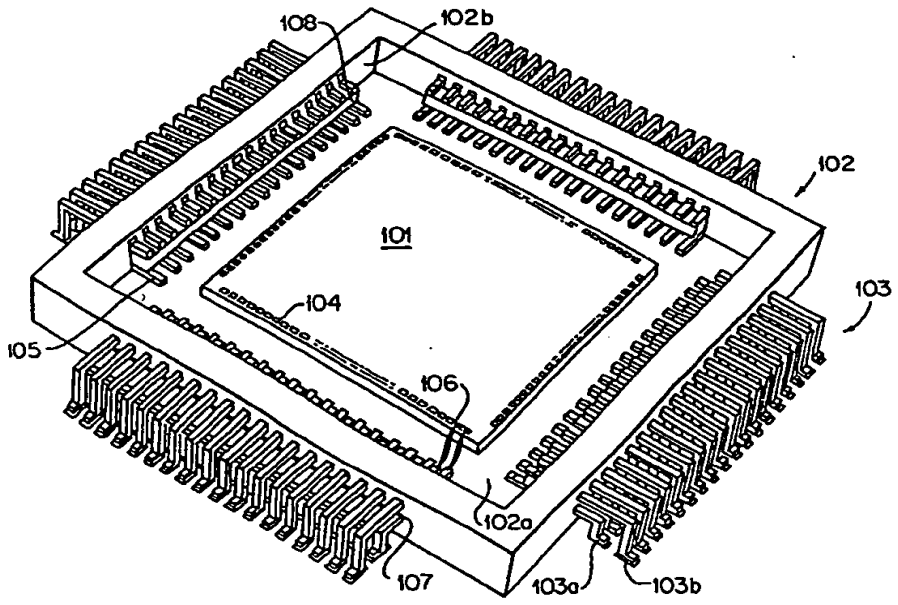

(57) Abstract

A semiconductor die carrier includes an insulative package; a plurality of conductive leads extending from the insulative package; a die attach plate housed within the insulative package, the die attach plate comprising a first surface located on one side of the die attach plate and a second surface located opposite the first surface on an opposing side of the die attach plate; at least one semiconductor die secured to the first surface of the die attach plate; and at least one semiconductor die secured to the second surface of the die attach plate.

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SEMICONDUCTOR DIE CARRIER HAVING DOUBLE-SIDED DIE ATTACH PLATE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. Patent Application Serial No. 08/208,586 to Stanford W. Crane, Jr. et al. filed March 11, 1994 and entitled PREFABRICATED SEMICONDUCTOR CHIP CARRIER, the content of which is relied upon and hereby expressly incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a prefabricated, peripherally-leaded, semiconductor die carrier having a reduced size yet still capable of supporting multiple semiconductor dies, and methods for making and using the semiconductor die carrier. In a preferred embodiment, the semiconductor die carrier has horizontally and vertically spaced rows of multiple leads, with each lead being assembled into the semiconductor die carrier as an individually manufactured lead rather than a sub-element of a lead frame, and also has a double-sided die attach plate configured to support the multiple semiconductor dies.

Description of the Related Art

Conventional package leads are typically configured for mounting using plated-through-hole (PTH) technology or surface-mount technology (SMT). In PTH technology, a conductive PTH is formed in a printed circuit board (PCB). Each lead of a package is inserted through a corresponding PTH and then soldered to form a solder joint fastening the

lead in conductive contact with the PTH. In SMT mounting, each lead of a package, rather than being soldered to extend through a PTH in a PCB, is soldered onto a conductive portion of a top surface of the PCB. A solder joint then maintains each lead of the leaded die carrier in a fastened relationship with respect to the PCB.

One type of SMT package is known as a QFP (Quad Flat Package). QFPs are typically manufactured using a molded plastic technology. Most QFPs are manufactured using a single-layer lead frame providing a single row of bent leads extending from each of the four sides of the QFP.

Multi-row lead configurations are also know. For example, it is known to provide two rows of leads, formed by using two different lead frames vertically spaced and insulated from each other, extending from sides of a QFP. It is also known to provide rows of multiple leads formed using vertically spaced lead frames with adjacent rows of leads primarily separated from each other by a gaseous dielectric such as air.

The aforementioned semiconductor die packages suffer from many deficiencies. Conventional semiconductor die packages, for example, are typically limited to a single semiconductor die per package. Thus, any signal traveling between multiple dies must cover a relatively long distance which, in turn, takes a relatively long period of time, thereby limiting computer speed and functionality. Furthermore, although single-die carriers are generally less expensive than multi-die carriers, the use of single-die carriers rather than multi-die carriers can result in an

overall increase in cost for the system in which they are being used.

Also, the molded plastic technology typically used to manufacture QFPs incorporates various processes following the wire bonding procedure which can have detrimental effects on the bonding integrity. Moreover, the use of lead frames during the manufacturing of QFP semiconductor packages and the like also results in numerous disadvantages.

From the foregoing, it can be understood that conventional semiconductor packages take up large amounts of board space and, related to this, separate semiconductor dies from one another by relatively long distances which take signals traveling between such dies a relatively long time to traverse; are expensive and often experience difficulties during manufacture; when of the single-die variety, can result in increased system costs; perform insufficiently due to procedures carried out after chip attachment and wire bonding that tend to inhibit bond integrity; and, after manufacture, are difficult, if not impossible, to repair. As a result of such limitations, current semiconductor packaging technology is not sufficient to meet the needs of existing and/or future semiconductor and computer technology. Semiconductor packaging technology has already failed to keep pace with silicon die technology, and as computer and microprocessor speeds continue to climb, with space efficiency being increasingly important, semiconductor die packages having even smaller area requirements will be required. The semiconductor die packages discussed above fall short of current and contemplated semiconductor and computer requirements.

SUMMARY OF THE INVENTION

Accordingly, it is a goal of the present invention to provide a prefabricated semiconductor die carrier occupying reduced amounts of board area, providing an increased number of contacts, decreasing the length of signal paths between semiconductor dies which communicate with one another through incorporation of multiple dies within a single die carrier, and capable of meeting the needs of existing and contemplated semiconductor and computer technology.

Another goal of the present invention is to provide a semiconductor die carrier manufactured without the use of lead frames and having leads extending from side portions thereof suitable for mounting using PTH technology, SMT methodology, or pluggable mounting.

Still another goal of the present invention is to provide a semiconductor die carrier that is fabricated and tested prior to placement of a semiconductor die within the carrier, thereby increasing final packaging yields and reducing total unit cost.

It is also a goal of the present invention to provide methods for making and using semiconductor die carriers having characteristics such as those discussed above.

These and other goals may be achieved by using a semiconductor die carrier comprising an insulative package; a plurality of conductive leads extending from the insulative package; a die attach plate housed within the insulative package, the die attach plate comprising a first surface located on one side of the die attach plate and a second surface located opposite the first surface on an opposing side of the die attach plate; at least one semiconductor die

secured to the first surface of the die attach plate; and at least one semiconductor die secured to the second surface of the die attach plate.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory, and are not restrictive of the invention as claimed. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the present invention and, together with the general description, serve to explain the principles of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of a two-tier embodiment of a prefabricated semiconductor die carrier in accordance with the present invention.

Fig. 2 is a perspective view of an SMT lead with an L-shaped foot portion configured in accordance with the present invention and positioned on a bonding pad of a multi-layer conductor such as a PCB.

Fig. 3 is a perspective view of a three-tier embodiment of a prefabricated semiconductor die carrier in accordance with the present invention.

Fig. 4 is a partial side view of a semiconductor die carrier including a cap, cavity-up configuration.

Fig. 5 is a partial side view of a semiconductor die carrier having a cavity-down configuration.

Fig. 6 is a partial side view of a semiconductor die carrier having a die indentation configuration and including a cap.

Fig. 7 is a partial side view of a semiconductor die carrier having a same or similar level configuration and including a cap.

Fig. 8 is a partial side view of a semiconductor die carrier having a platform configuration and including a cap.

Fig. 9 is a partial perspective view of a four-tier embodiment of a prefabricated semiconductor die carrier in accordance with the present invention.

Fig. 10 is a perspective view of a multi-die configuration of a prefabricated semiconductor die carrier in accordance with the present invention.

Fig. 11 is a side view of a semiconductor die carrier having a cavity-down configuration.

Fig. 12 is a close-up view of a portion of the semiconductor die carrier depicted in Fig. 11.

Fig. 13 is a top view of a cavity portion of the semiconductor die carrier depicted in Fig. 11 having a diagram of multiple semiconductor dies superimposed thereon.

Fig. 14 is a side view of a semiconductor die carrier comprising a die attach plate having multiple sides each supporting at least one semiconductor die.

Fig. 15 is a close-up view of a portion of the semiconductor die carrier depicted in Fig. 14.

Fig. 16 depicts a pair of flowcharts comparing a conventional manufacturing method with a method in accordance with the present invention performed in order to manufacture, transport, and mount a prefabricated semiconductor die carrier.

Fig. 17 depicts a flowchart representing preferred method steps in accordance with the present invention

relating to the manufacture and shipping of a semiconductor die carrier incorporating a double-sided die attach plate.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

A prefabricated semiconductor die carrier in accordance with the present invention includes a double-sided die attach plate with at least one semiconductor die secured to each side of the plate, and has multiple rows of electrically conductive leads arranged at vertically spaced multiple levels around the periphery of the carrier. Each of the leads is manufactured and assembled into the semiconductor die carrier prior to the die attach step as an individually manufactured lead, rather than as a sub-element of a lead frame, to facilitate the multiple-row, multiple-level structure.

The leads of the semiconductor die carrier extend into the die carrier through the side walls of the die carrier, forming a series of vertically spaced rows of multiple leads around the semiconductor die. The portions of the leads extending through the side walls have wire bond terminals formed thereon. A wire bond insulator may be used to separate the rows of leads. The semiconductor die can be mounted within the carrier with the peripheral pads of the die facing up and away from the PCB, in a cavity-up configuration, or with the peripheral pads of the die facing down toward the PCB, in a flip-chip or cavity-down configuration. In a preferred multiple-die embodiment, at least one semiconductor die is mounted on an upper surface of a die attach plate with the peripheral pads facing up and away from the PCB, and at least one semiconductor die is

mounted on a lower surface of the die attach plate with the peripheral pads facing down toward the PCB.

Encapsulation for the semiconductor die carrier of the present invention is performed by filling the die cavity with an epoxy, a liquid crystal polymer such as HYSOL (a trademark of Dexter) or similar or other high-temperature material. Alternatively, the semiconductor die carrier may be capped with a plastic component or thermally conductive cap that serves as a heat sink.

The semiconductor die carrier of the present invention provides a package having a reduced size as compared to known semiconductor packages, yet increases the number of interconnects available for the designer and user. The die carrier may be configured to be pluggable, compatible with the PTH technology, or compatible with the SMT methodology. The semiconductor die carrier is prefabricated and tested prior to introduction of the semiconductor die to the carrier, thereby increasing finished product yields and reducing total unit cost. The configuration of the die carrier allows the semiconductor die to be bonded from multiple rows of pads on the die to multiple levels of vertically spaced rows of leads while maintaining a very low profile for the die carrier.

Details relating to the present invention will now be discussed with reference to the accompanying drawings. For the sake of convenience, the same reference numerals will be used to designate the same or similar components of the present invention throughout the accompanying drawings.

A perspective view of an embodiment of a prefabricated semiconductor die carrier in accordance with the present

invention is shown in Fig. 1. In accordance with the embodiment of Fig. 1, the semiconductor die carrier includes a semiconductor die 101; an insulating substrate 102, having a floor 102a and a plurality of side walls 102b; a plurality of leads 103, including lower leads 103a and upper leads 103b; a plurality of bonding pads 104 formed on the semiconductor die; a plurality of bonding terminals 105 formed on the leads 103, respectively; and a plurality of bonding wires 106 each connecting at least one of the bonding pads 104 of the die to a corresponding one of the bonding terminals 105 formed on the leads.

The insulating substrate 102 of the semiconductor die carrier is made of a liquid crystal polymer or material having properties the same or similar to a liquid crystal polymer. Preferably, the liquid crystal polymer for the insulating substrate 102 is VECTRA (trademark), which has a coefficient of thermal expansion that is approximately the same as or similar to the coefficient of thermal expansion for silicon.

The insulating substrate 102 may be formed in a molding process carried out prior to inserting the leads 103 into the side walls 102b of substrate, and prior to mounting the die 101 onto the floor 102a of the substrate. During the molding process, a series of lead holes or passages 107 are molded within the side walls 102b of the substrate, each of the passages for receiving a corresponding one of the leads 103, and a series of ledges 108 are formed inside the side walls of the substrate around the periphery where the die is to be placed. The ledges 108 serve to support the leads 103 (during the wire bonding procedure, for example). As an

alternative to forming the lead passage 107 and ledges 108 during the molding process, the lead passages and/or ledges could be added after molding by, for example, removing material of the substrate to form the lead passages and/or by applying insulative material (using an adhesive or epoxy, for example) to form the ledges.

In the embodiment of Fig. 1, the lower leads 103a and upper leads 103b are aligned in a straight line with respect to one another than staggered. In other words, for each upper lead 103b, a corresponding lower lead 103a is positioned directly beneath that upper lead. While not shown in Fig. 1, the lower leads 103a and upper leads 103b could be staggered with respect to one another. In a staggered configuration, none of the lower leads 103a would be beneath any of the upper leads 103b. Instead, progressing along a given one of the side walls 102b, every other lead would be a lower lead 103a or an upper lead 103b.

A perspective view of an example of one of the leads 103 is shown in Fig. 2. As seen from Fig. 2, each of the leads 103 includes a bonding extension section 1031 having a bonding terminal 105 formed on an end portion thereof; a stabilizing section 1032; and an external lead section 1033. Each lead 103 may be formed of beryllium copper, phosphor bronze, brass, a copper alloy, tin, gold, palladium, or any other suitable metal or conductive material, and the bonding terminal 105 may be a gold-plated pad or pad formed of another suitable conductive material.

The bonding extension section 1031 is a relatively long and narrow portion of the lead 103 which protrudes toward the interior of the semiconductor die carrier from the inner

surface of a corresponding one of the side walls 102b. The bonding terminal 105 may be, for example, a bonding pad to which a bonding wire 106 for attachment to a corresponding bonding pad 104 on the die 101 can be connected.

The stabilizing section 1032 of each lead 103 is the portion of the lead that is anchored within a side wall 102b of the substrate 102. The stabilizing section has a larger cross-sectional area than that of the bonding extension section 1031 and may also have a larger cross-sectional area than that of the external lead section 1033. The thick stabilizing section retains the lead and prevents forces exerted on the external lead section from transferring to the bonds associated with bonding wire 106.

The external lead section 1033 includes a horizontally-extending section 1033a, a corner section 1033b, a vertically-extending section 1033c, and a foot section 1033d. The configuration and length of the horizontally-extending and vertically-extending sections for each individual lead 103 are selected based on design requirements and, in particular, based on whether that lead will be used as a lower lead 103a or an upper lead 103b.

Dimensions of the semiconductor die carrier having two vertically spaced rows of multiple leads can be understood, for example, with reference to the accompanying figures.

As can be seen from Fig. 1, for example, a two-row semiconductor die carrier in accordance with the present invention may have, for example, a height of 2.0 mm, a width of 17.9 mm, and a lead row length of 8.7 mm. In this configuration, the semiconductor die carrier of the present invention can be manufactured to be approximately 64% smaller

than conventional 128 pin QFPs, and at the same time provides 16 extra leads.

From Fig. 2, it can be understood that a lead 103 in accordance with the present invention may have a bonding extension section 1031 that is 1.5 mm in length; a stabilizing section 1032 that is 1.0 mm in length, and an external lead section 1033 having a vertically-extending section 1033c that varies in length depending whether the lead is an upper lead or a lower lead. As shown in Fig. 2, the foot section 1033d of a lead 103 configured for mounting in accordance with SMT can have a cross-section of 0.2 x 0.4 mm, for example, for mounting on an SMT solder joint 109 of a PCB having an exemplary cross-section of 0.4 x 0.6 mm.

A perspective view of another embodiment of a prefabricated semiconductor die carrier in accordance with the present invention is shown in Fig. 3. The embodiment of Fig. 3 essentially corresponds to the embodiment shown in Fig. 1, except that three vertically spaced rows of multiple leads 103a, 103b, and 103c are used instead of two of such rows. Such a configuration enhances the interconnect capabilities of the semiconductor die carrier. While not shown in Fig. 3, ledges 108 might be applicable to the three-row semiconductor die carrier in accordance with the present invention.

The semiconductor die carrier of Fig. 3 may be manufactured in the same manner that the carrier shown in Fig. 1 is manufactured. Exemplary dimensions for the embodiment of Fig. 3 are a height of 2.7 mm; a width of 21.5 mm; and a lead row length of 11.8 mm. In this configuration, the semiconductor die carrier of Fig. 3 can be configured to

provide 208 leads using approximately half of the area (for example, board area) of that required by conventional QFP technology.

A partial side view of the embodiment of Fig. 13 is shown in Fig. 4. The illustration of Fig. 4 shows features of the semiconductor die carrier including a die bond adhesive 111 for mounting the die 101 on the floor 102a; bonding wires 106 which, in each of the embodiments of the present invention, may be dimensioned to have a wire length of less than 1.0 to 2.5 mm, for example; a cavity filler 112 used to fill the cavity defined by the floor 102a and side walls 102b of the carrier during the encapsulation process; and a sealing cap 113, made of plastic or other thermally-conductive material such as metal or VECTRA (trademark), and capable of functioning as a heat sink, for providing a cover for the semiconductor die carrier.

Figs. 5-8 show various configurations relating to the placement of the semiconductor die 101 within the semiconductor die carrier. Although Figs. 5-8 depict an embodiment having three-row configuration, it should be noted that the die placement configurations illustrated in these figures are also applicable to the other embodiments of the present invention, including the one-row and two-row embodiments discussed above and the four-row embodiments discussed below.

Where Fig. 4 corresponds to a cavity-up configuration, in which the semiconductor die is mounted within the carrier with the peripheral pads of the die facing up and away from the PCB or other mounting surface, Fig. 5 corresponds to a cavity-down or flip-chip configuration, in which the

peripheral pads of the die face down toward the PCB or other interface surface. In the configuration of Fig. 5, the die 101 is mounted on a heat sink cap 114, preferably formed of a thermally conductive material, and then wire bonding, encapsulation, and sealing using a sealing cap 113, preferably formed of VECTRA (trademark), take place. The heat sink cap 114 can be an integrally molded component of the substrate 102, or attached to the substrate 102 after molding of the substrate is completed.

Fig. 6 shows that the semiconductor die 101 may be embedded or placed into an indentation, similar to the size of the semiconductor die, formed in the floor 102a for receipt of the die. In this configuration, the top surface of the die is located below the bonding extension sections 1031 of the lower leads 103a.

Fig. 7 shows the placement of the semiconductor die 101 on top of a flat floor 102a. In this configuration, the top surface of the semiconductor die 101 is the same level or similar in height to the height of the bonding extension sections 1031 of the lower leads 103a.

Fig. 8 shows the placement of the semiconductor die 101 on a raised platform 115, similar to the size of the die, formed in the interior of the semiconductor die carrier. The raised platform 115 may be an integrally molded component of the substrate 102, or attached to the substrate 102 after molding of the substrate is completed.

It should be noted that, in each of the configurations shown in Figs. 5-8, the semiconductor die 101 may be mounted using an adhesive material, epoxy, or the like.

A partial view of another embodiment of a preferred semiconductor die carrier in accordance with the present invention is shown in Fig. 9. The embodiment of Fig. 9 essentially corresponds to the embodiments shown in Figs. 1 and 3, for example, except that four vertically spaced rows of multiple leads 103a, 103b, 103c, and 103d are used instead of two or three of such rows. Such a configuration further enhances the interconnect capabilities of the semiconductor die carrier. Fig. 9 illustrates that, in all the embodiments of the present invention, the stabilizing section 1032 of each lead 103 may overlap or extend beyond the inner surface of its corresponding side wall 102b, if desired. Alternatively, in all of the embodiments of the present invention, a stop could be used to prevent over-insertion of the leads.

The semiconductor die carrier of Fig. 9 is manufactured in the same manner that the die carriers shown in Figs. 1 and 3 are manufactured. Exemplary dimensions for the embodiment of Fig. 9 are a height of 3.4 mm; a width of approximately 28.0 mm; and a lead row length of 16.2 mm. In this configuration, the semiconductor die carrier of Fig. 9 can be manufactured to be approximately 57% smaller than conventional 304-pin QFPs.

The previously-discussed embodiments and configurations in accordance with the present invention contemplate a prefabricated semiconductor die carrier having one row of multiple leads or two, three, or four vertically spaced rows of multiple leads. While not shown in the accompanying drawings, in accordance with the present invention, prefabricated semiconductor die carriers having five or more

vertically spaced rows of multiple leads are also contemplated. Such prefabricated semiconductor die carriers are considered to be within the spirit and scope of the present invention.

Fig. 10 is a perspective view of another aspect of the present invention that is applicable to all of the previously-discussed embodiments. As can be seen from Fig. 10, a plurality (e.g., four) of semiconductor dies 101 may be incorporated within a prefabricated semiconductor die carrier in accordance with the present invention, thus allowing an even more efficient usage of materials and board space. In Fig. 10, a multi-layer ceramic component 122, having a plurality of levels of electrically conductive material therein, is glued or otherwise adhered to the floor 102a, and the plurality of semiconductor dies 101 are glued or otherwise adhered to the multi-layer ceramic component. The dies may or may not be electrically connected to the multi-layer ceramic component using C4, wire bond, TAB, or other bonding technologies. In the case where C4, TAB, or like bonding is used, conductive lands on the bottom surface of the dies are used to provide electrical interconnection between the dies and the ceramic component 122. In the case where wire bonding is used, bonding wires (now shown) connected at one end to the bonding pads 104 and at the other end to the ceramic component 122 are used to provide electrical interconnection between the dies and the ceramic component.

The leads 103 are either soldered to the ceramic component 122, or electrically connected to the ceramic component using bonding wires (not shown). For the bonding

pads 104 along the outwardly-facing edges of each semiconductor die 101, rather than transmitting the signals between the leads 103 and the bonding pads 104 via the multi-layer ceramic component 122, such signals may be transmitted directly between the bonding pads and leads via bonding wires (not shown) directly connected to the leads 103 at one end and directly connected to the bonding pads 104 at the other end.

While Fig. 10 shows the incorporation of four semiconductor dies within a single prefabricated semiconductor die carrier in accordance with the present invention, either more or less dies per semiconductor die carrier are contemplated. As stated previously, the incorporation of a plurality of semiconductor dies within a single die carrier allows more effective usage of materials and board space.

Although the semiconductor die carrier of Fig. 10 advantageously incorporates a plurality of semiconductor dies within a single semiconductor die carrier, the semiconductor die carrier of Fig. 10 takes up more board area than a semiconductor die carrier including only a single die, due to the side-by-side placement of multiple dies therein. To overcome this disadvantage, the inventors have considered incorporating multiple semiconductor dies in a 320-lead semiconductor die carrier having a cavity-down or flip-chip configuration such as that depicted in Figs. 11 and 12. More particularly, the inventors have considered incorporating multiple dies within the square die cavity 116 of the cavity-down or flip-chip configuration of Figs. 11 and 12. As depicted in Fig. 13, however, while there is enough room in

square cavity 116 to accommodate a single square semiconductor die, there is not enough room in the square cavity to accommodate more than one square semiconductor die (e.g., a first square semiconductor 101a and a second squar semiconductor die 101b). If one attempted to place two such semiconductor dies within square cavity 116, such placement would not be possible due to the overlap between the square semiconductor dies 101a and 101b illustrated in Fig. 13.

The embodiment of Figs. 14 and 15 solves this dilemma by moving the die attach plate 117 down so that it lines up with one of the steps of the semiconductor die carrier (e.g., the lower step separating the row of leads 103a from the row of leads 103b). Relocating the die attach plate 117 in this matter creates two cavities, that is, a first cavity 116a and a second cavity 116b, thus doubling the die attach area of the plate. Such a configuration allows one or more semiconductor dies 101a to be secured to the top surface of die attach plate 117, and one or more semiconductor dies 101b to be secured to the bottom surface of the die attach plate, with the dies 101a and 101b being attached to the leads of the semiconductor die carrier by bonding wires 106a and 106b, respectively. A further result of this configuration is that, in the same amount of module area occupied by the single-die configuration of Figs. 11 and 12, the configuration of Figs. 14 and 15 can accommodate multiple dies mounted back-to-back on either side of the semiconductor die attach plate.

In accordance with the embodiment of Figs. 14 and 15, die attach plate 117 may be an electrically insulative plate electrically insulating upper semiconductor 101a from lower

semiconductor 101b or, alternatively, it may be multi-layered conductor such as a mini-PCB with internal wiring allowing signals to travel between the upper and lower dies via the die attach plate. Each of the semiconductor dies may be electrically connected to the multi-layer conductor by bonding wires, C4, TAB, or the like. In the case where die attach plate 117 is an electrically insulating plate, signals can be transferred between upper semiconductor die 101a and lower semiconductor die 101b off-module at the PCB level by way of bonding wires 106a and 106b and one or more of leads 103 (e.g., leads 103a and 103c). In the case where die attach plate 117 is a multi-layer conductor, on the other hand, signals can be transferred between upper semiconductor die 101a and lower semiconductor die 101b either off-module at the PCB level in the same way as when the die attach plate is an insulating plate, or within the module directly via the conductive paths within the die attach plate, or both. Figs. 14 and 15 show that when die attach plate 117 is a multi-layer conductor, the die attach plate can be provided with its own set of bonding wires 106c to allow a further transmission path to the PCB via the leads in addition to those provided by bonding wires 106a and 106b.

Due at least in part to the proximity between semiconductor dies 101a and 101b in the configuration of Figs. 14 and 15, this embodiment is preferably to be used in low power environments (e.g., 4 watts or less). Thus, the embodiment of Figs. 14 and 15 is ideally suited for use as a controller chip and/or non-volatile flash memory chip having a capacity of, or example, 4 megabytes. In other words, in the embodiment of Figs. 14 and 15, semiconductor dies 101a

and 101b can both be microprocessor or other such controller dies or, alternatively, both may be memory dies. In a preferred embodiment, one of semiconductor dies 101a and 101b comprises a microprocessor die while, at the same time, the other of semiconductor dies 101a and 101b comprises a memory die.

Although a large portion of this text is devoted to the discussion of the situation where elements 101a and 101b are semiconductor dies, it should be noted that either or both of elements 101a and 101b may alternatively be any type of active or passive electronic component (such as a piezoelectric crystal, an oscillator, or a capacitor, for example) other than a semiconductor die. Thus, in the embodiment of Figs. 14 and 15, elements 101a and 101b can both be a semiconductor die or, alternatively, both can be one of a passive or active electric component other than a semiconductor die or, alternatively, one of elements 101a and 101b may be a semiconductor die while the other is a passive or active electronic component other than a semiconductor die. In one preferred embodiment, one of components 101a and 101b comprises a piezoelectric crystal while, at the same time, the other of components 101a and 101b comprises a tuning capacitor.

The incorporation of a plurality of semiconductor dies within single semiconductor die carrier in the manner of Figs. 14 and 15 not only allows more effective usage of materials and board space, but also can increase computer speeds due to the close proximity of communicating semiconductor dies with one another. It should be noted that although Figs. 14 and 15 show the use of a double-sided die

attach plate incorporated within a three-tier semiconductor die carrier, the double-sided die attach plate concept is also applicable to semiconductor die carriers having one, two, four, five, or more vertically spaced rows of leads.

Fig. 16 includes two flowcharts. The flowchart at the left illustrates steps performed in the manufacturing of a conventional molded plastic semiconductor package. The flowchart at the right illustrates steps performed in a manufacturing process for producing a prefabricated semiconductor carrier in accordance with the present invention. As can be seen from Fig. 16, the present invention entails fewer steps following the die bond procedure as compared to conventional manufacturing processes. Most notably, the molding, mold cure, deflash, shear, lead electroplate, lead trim and form, and solder dip steps of the conventional manufacturing process are completely absent from the manufacturing process of the present invention following die bonding. The result is that the costly yield losses associated with the conventional process are completely avoided by the manufacturing process of the present invention.

In accordance with the present invention as depicted in the rightward flowchart of Fig. 16, in a step S1, the substrate 102, including the floor 102a and side walls 102b and, if desired, lead passages 107 and ledges 108, are integrally formed using a molding process. As an alternative to forming the lead passages 107 and ledges 108 during the molding process, the lead passages and/or ledges could be added after molding by, for example, removing material of the substrate to form the passages and/or by applying insulative

material (using an adhesive or epoxy, for example) to form the ledges. Components such as die attach plate 117 could also be formed either integrally during the molding process, or such elements could be added after molding. Moreover, it is envisioned that rather than being formed integrally in a single molding process, the floor 102a and side walls 102b could be molded separately, and then fastened together using an epoxy or other adhesive. The use of VECTRA (trademark) as the material for the substrate allows the parts of the semiconductor die carrier to be molded and assembled with a high degree of accuracy. As an alternative to forming the substrate 102 and then inserting the leads into the substrate, the substrate could be formed around the leads in an insert molding process.

In a step S2, the leads 103 are formed. The lead formation step S2 entails punching or stamping out individual leads from strips or drawn wire using, for example, a die. The inventors have found that by individually manufacturing each lead 103, rather than using a lead frame to manufacture such leads, manufacturing costs are reduced and, at the same time, yield is increased.

The aforementioned lead-manufacturing methods allow for selective plating and automated insertion. The leads for stamping can either be loose, on a bandolier carrier 129 or on a strip since the asymmetrical shape lends itself to consistent orientation in automated assembly equipment. The different length external lead sections assist with orientation and vibratory bowl feeding during automated assembly. The present invention is compatible with both stitching and gang-insertion assembly equipment. The

insulative components have been designed to facilitate automatic and robotic insertion onto PCBs or in termination of wire to connector.

Step S3 of Fig. 16 involves inserting the leads 103 into the side walls 102b of the substrate 102. In the situation where the floor 102a and the side walls 102b are formed separately and then fastened together at a later time, the leads may be inserted into the side walls before they are fastened to one another or to the floor. Each of the leads 103 is inserted into a corresponding one of the lead passages 107 in the side walls 102b. The dimensions of the leads 103 and lead passages 107 are such that each lead fits tightly within it corresponding lead passage 107. However, if desired, each lead 103 can be further fastened within its corresponding lead passage 107 and/or onto a corresponding ledge 108 using an epoxy or other adhesive material.

It should be kept in mind that rather than forming the substrate and then inserting the leads into the side walls of the substrate, placement of the leads 103 with the side walls 102b of the substrate may be accomplished using an insert molding process. Insert molding is applicable to all embodiments of the present invention.

In step S4, mechanical testing is performed to ensure that the leads 103 are securely fastened within the substrate 102; to ensure that coplanarity of the leads 103 falls within an acceptable range; to ensure that each lead is aligned properly within its respective lead passage; and the like. Also, electrical testing is performed to ensure that signals can be transmitted properly through the leads of the carrier to the exterior of the carrier, and vice versa; and to ensure

that none of the leads are shorted or would be likely to short during subsequent stages of the manufacture and usage of the semiconductor die carrier. In accordance with step S5, the substrate 102 having leads 103 disposed therein is packaged and then shipped to the place where a semiconductor die, manufactured in step S6, will be bonded to the substrate.

Step S7 of Fig. 16 involves attaching the semiconductor die 101 to floor 102a or another support surface (for example, raised platform 115 or die attach plate 117) within the semiconductor die carrier. In the case where multiple dies are to be incorporated into the semiconductor die carrier, such as in the embodiment depicted in Figs. 14 and 15, a first one of the dies is attached to the die plate and thereafter electrically tested, a second one of the dies is then attached to the die plate and thereafter electrically tested, and so on. The attachment may be carried out using an adhesive, an epoxy or the like.

Step S8 entails a bonding procedure wherein a bonding wire 106 is connected between components of a pair including a bonding pad 104 on the die 101 and a bonding terminal 105 on one of the leads 103. The bonding wires allow electrical connection between the die 101 and the various leads 103.

In step S9, further electrical tests may be performed to provide additional assurance that an acceptable product is being manufactured. In step S10, encapsulation is performed by filling the cavity defined by the floor 102a and the side walls 102b of the substrate 102 with epoxy, a liquid crystal polymer such as VECTRA (trademark), or other high-temperature material. Then the semiconductor die carrier may capped with

a plastic component or thermally-conductive cap that may serve as a heat sink, and thereafter sealed, although use of a cap is optional. It should be noted that when a cap is used, the aforementioned encapsulation step becomes optional. The heat sink and/or high-temperature material which may be used for encapsulation and sealing facilitate the heat dissipation capabilities of the semiconductor die carrier. In step S11, further mechanical and electrical quality control testing may be performed to increase the likelihood that the semiconductor die carrier will function as expected.

In accordance with step S12, the completed semiconductor die carrier is packaged and shipped to the customer. Preferably, the semiconductor die carrier is packaged and shipped to the customer using the same transportation package it was received in.

Step S13 relates to the mounting of the finished semiconductor die carrier on or within an interface surface such as a PCB surface. In step S13, either PTH technology or SMT methodology may be used to accomplish PCB interfacing or, alternatively, the carrier may be plugged into a pluggable socket mounted on a PCB or other interface device. The configurations of the footprints of the semiconductor die carrier (or of the pluggable socket, if one is used) facilitate the routing of traces on the PCB or other interface surface onto or within which the semiconductor die carrier is being mounted. Further mechanical and electrical testing can be performed after the mounting process is completed.

Further details on a preferred way in which step S7 (die bond) through step S13 (mount on PCB) of Fig. 16 may be

carried out for a double-sided semiconductor die carrier such as that depicted in Figs. 14 and 15 can be understood from the flowchart in Fig. 17. With reference to Figs. 14 and 15, in the method steps of Fig. 17 a first one of semiconductor dies 101a and 101b is attached to a first side of die attach plate 117 (step S21 of Fig. 17), wire bonded thereto (step S22), and then tested (step S23). Steps S21 and S22 could alternatively be accomplished via C4, TAB, or some other die attach/bonding procedure. If the test in step S23 is failed, then the module is reworked or scrapped (step S24). Consequently, it is recommended that the side being the least complicated and having the least cost be tested first, so as to reduce waste and expense.

If the test in step S23 is passed, the first side is potted (step S25), the module is flipped over to its second side (step S26), a second one of semiconductor dies 101a and 101b is attached to the second side of die attach plate 117 (step S27), wire bonded thereto (step S28), and then the entire module is tested (step S29). As with steps S21 and S22, steps S27 and S28 could alternatively be accomplished via C4, TAB, or some other die attach/bonding procedure. If the module fails the test of step S29, it is reworked or scrapped (step S30). If, on the other hand, it passes that test, the second side of the module is potted (step S31) and then the module is subjected to final testing (step S32). Depending on whether the module passes the final test of step S32, it is either scrapped (step S33) or shipped (S34).

As compared to conventional methods, there are significantly fewer production steps involved in producing a semiconductor die carrier in accordance with the present

invention. The semiconductor die carrier of the present invention begins as a pre-formed platform into which the die is inserted. Encapsulation is then accomplished by capping and sealing the platform after it has been tested. This results in the elimination of the entire molding, bending, and clean-up processes and the related bonding of the carrier. Because the leads of the present invention are pre-formed and inserted into the plastic platform, they are undisturbed by additional procedures conventionally performed after the die is introduced into the semiconductor package. In the conventional process, the most sensitive aspects of the manufacturing process, encapsulating the die and electroplating and forming the leads, are performed after the die and the semiconductor package have been mated. This results in comparatively costly scrap, which may be due to lack of coplanarity among the leads, breakage, wire bond failure due to high-pressure molding, or other problems. All of these problems result in sacrificing the die as well as the package. The semiconductor die carrier of the present invention, however, could be delivered to the die attach area completely tested for plating, mechanical integrity, and dimensional characteristics, and the die need only be inserted into packages meeting acceptable quality standards. The elimination of the intermediate processes also reduces labor costs.

The semiconductor due carrier of the present invention can be configured with a precise number of leads easier than current designs due to the programmable nature of its assembly. A designer can specify varied numbers of leads or changes in package size, without the need to design and

manufacture new lead frame configurations. With the present invention, both the number of leads on a side of a package, and the number of rows of leads, can be varied simply by producing a new mold for the prefabricated platform and reprogramming the lead insertion equipment to vary the number of leads or lead configuration.

As discussed above, the present invention provides many advantages over conventional packaging technology. Such advantages include the provision of a semiconductor die carrier occupying reduced amounts of board area, providing an increased number of leads, decreasing the length of signal paths between semiconductor dies through incorporation of multiple dies within a single die carrier, and capable of meeting the needs of existing and contemplated semiconductor and computer technology. The advantages provided by the present invention over conventional packaging technology illustrate that the present invention, unlike conventional packaging technology, is capable of keeping pace with the rapid advances that are currently taking place in the semiconductor and computer technologies.

It will be apparent to those skilled in the art that various modifications and variations can be made in the disclosed process and product without departing from the scope or spirit of the invention. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and example be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor die carrier comprising:

an insulative package;

a plurality of conductive leads extending from the insulative package;

a die attach plate housed within the insulative package, the die attach plate comprising a first surface located on one side of the die attach plate and a second surface located opposite the first surface on an opposing side of the die attach plate;

at least one semiconductor die secured to the first surface of the die attach plate; and

at least one semiconductor die secured to the second surface of the die attach plate.

2. The semiconductor die carrier according to claim 1, wherein the die attach plate comprises a insulative member electrically insulating the at least one semiconductor die secured to the first surface of the die attach plate from the at least one semiconductor die secured to the second surface of the die attach plate.

3. The semiconductor die carrier according to claim 1, wherein the die attach plate comprises a multi-layer conductor providing a signal path between the at least one semiconductor die secured to the first surface of the die attach plate and the at least one semiconductor die secured to the second surface of the die attach plate.

4. The semiconductor die carrier according to claim 1, further comprising means for electrically connecting at least one of the plurality of conductive leads to the at least one semiconductor die secured to the first surface of the die attach plate, and means for electrically connecting at least one of the plurality of conductive leads to the at least one semiconductor die secured to the second surface of the die attach plate.

5. The semiconductor die carrier according to claim 1, wherein the insulative package comprises a top surface, a bottom surface, and a plurality of side surfaces coupling the top surface and the bottom surface, and the plurality of conductive leads comprises multiple leads extending out from each of the side surfaces of the insulative package.

6. The semiconductor die carrier according to claim 1, wherein the plurality of conductive leads comprises multiple vertically-spaced rows of leads extending out from the side surfaces of the insulative package.

7. The semiconductor die carrier according to claim 1, wherein each of the conductive leads is individually manufactured without use of a lead frame.

8. The semiconductor die carrier according to claim 1, wherein at least one of the semiconductor dies is a microprocessor die.

9. The semiconductor die carrier according to claim 1, wherein at least one of the semiconductor dies is a microprocessor die and at least one of the semiconductor dies is a memory die.

10. The semiconductor die carrier according to claim 1, wherein the die attach plate separates a space within the insulative package into a first cavity and a second cavity, the at least one semiconductor die secured to the first surface is located in the first cavity, and the at least one semiconductor die secured to the second surface is located in the second cavity.

11. An electronic component carrier comprising:

an insulative package;

a plurality of conductive leads extending from the insulative package;

an attachment plate housed within the insulative package, the attachment plate comprising a first surface located on one side of the attachment plate and a second surface located opposite the first surface on an opposing side of the attachment plate;

at least one electronic component secured to the first surface of the die attach plate; and

at least one electronic component secured to the second surface of the die attach plate.

12. The electronic component carrier according to claim 11, wherein at least one of the electronic components is a piezoelectric crystal.

13. The electronic component carrier according to claim 11, wherein at least one of the electronic components is a capacitor.

14. The electronic component carrier according to claim 11, wherein at least one of the electronic components is a piezoelectric crystal and at least one of the electronic components is a tuning capacitor.

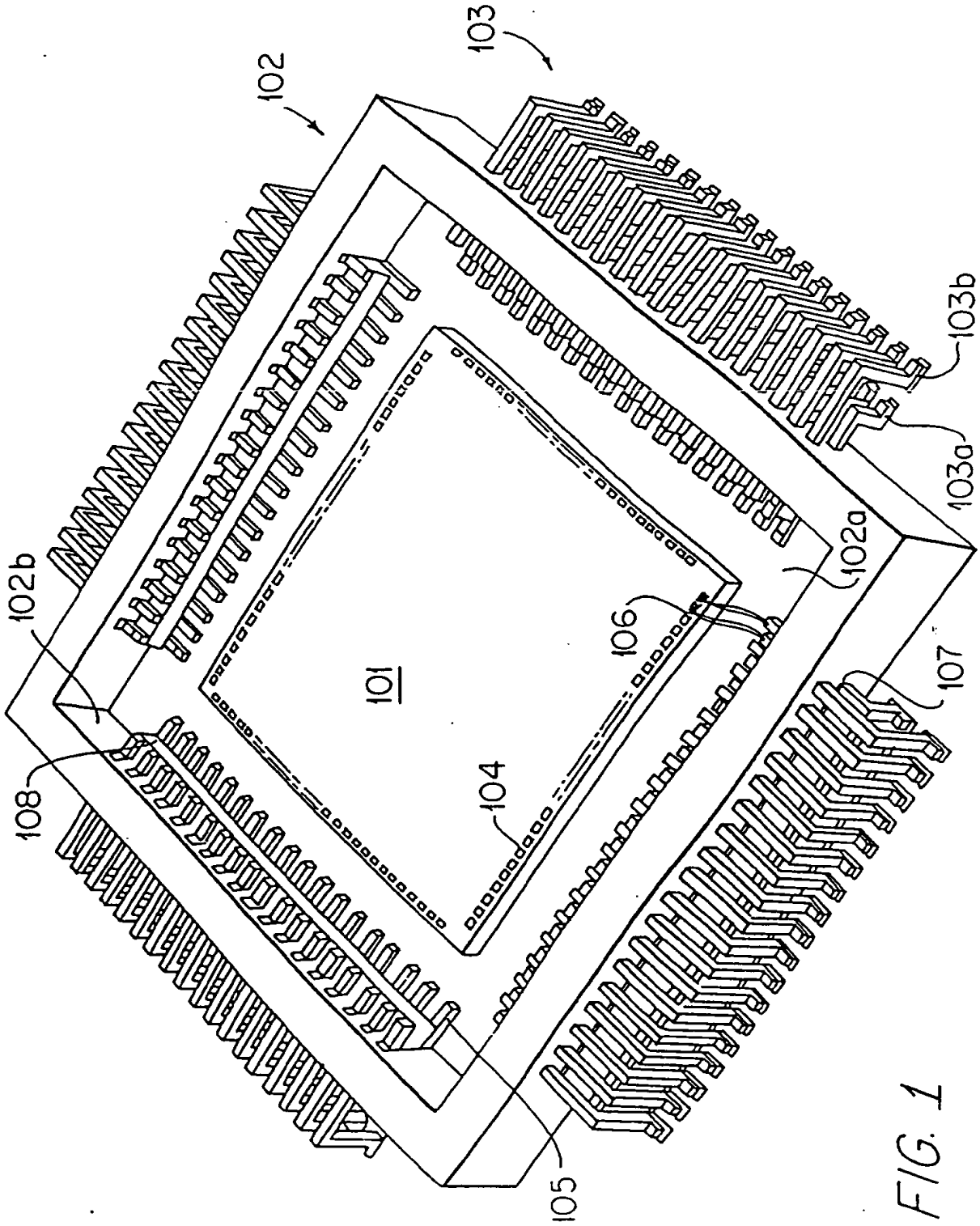

FIG. 1

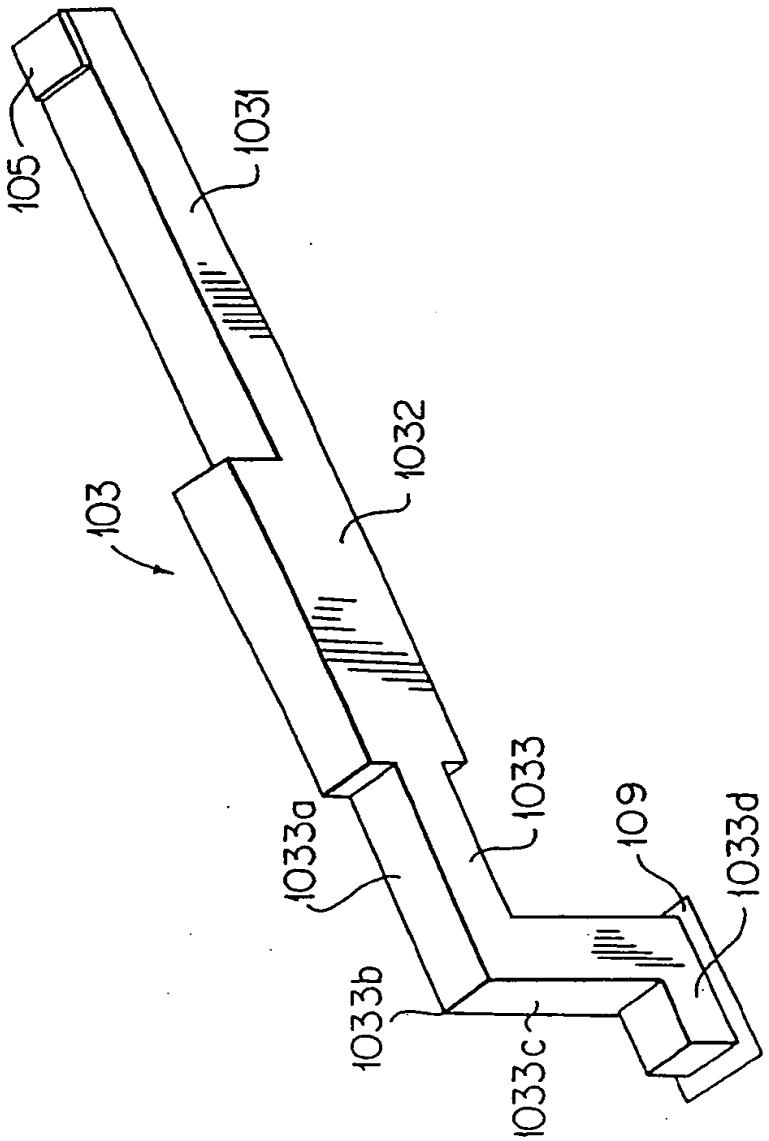

FIG. 2

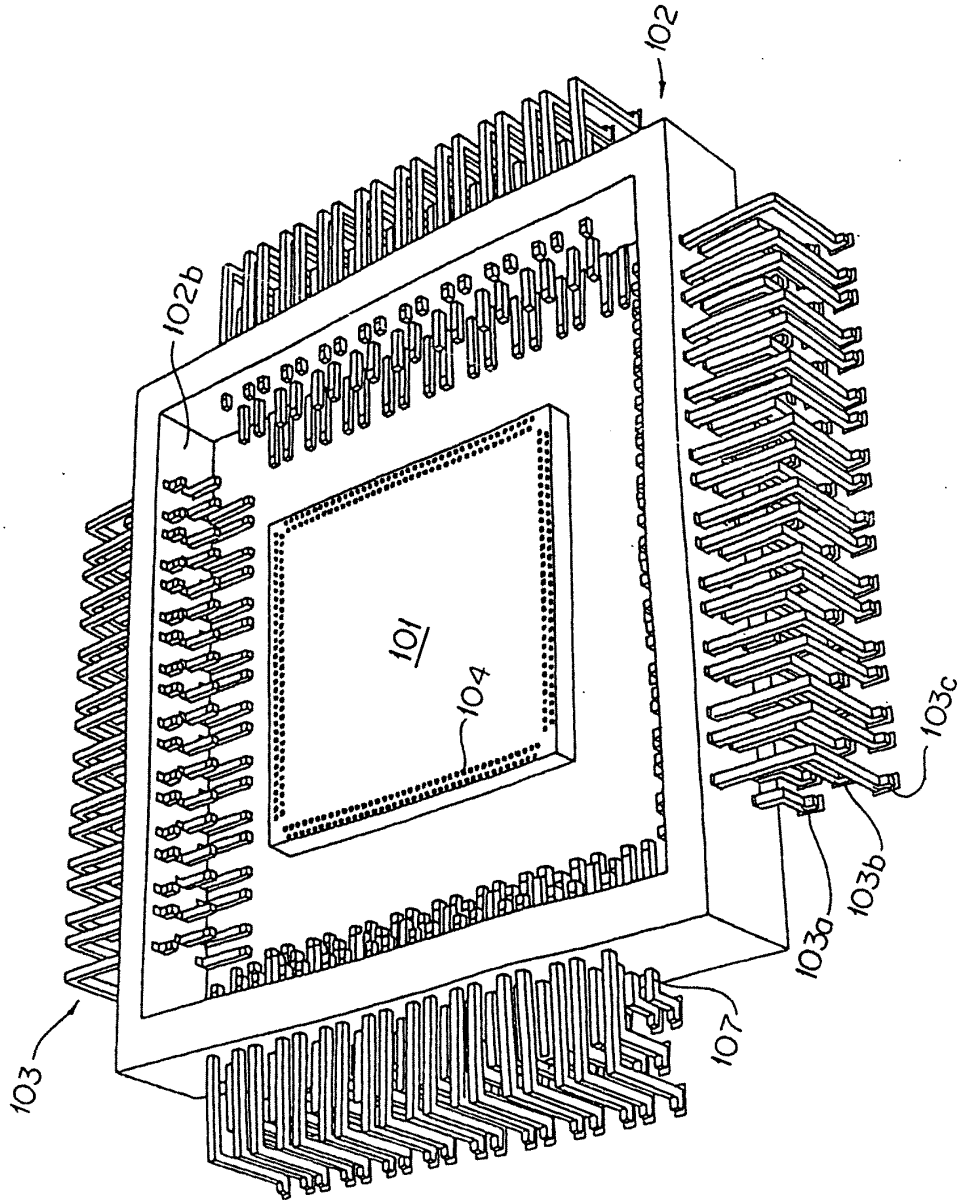

FIG. 3.

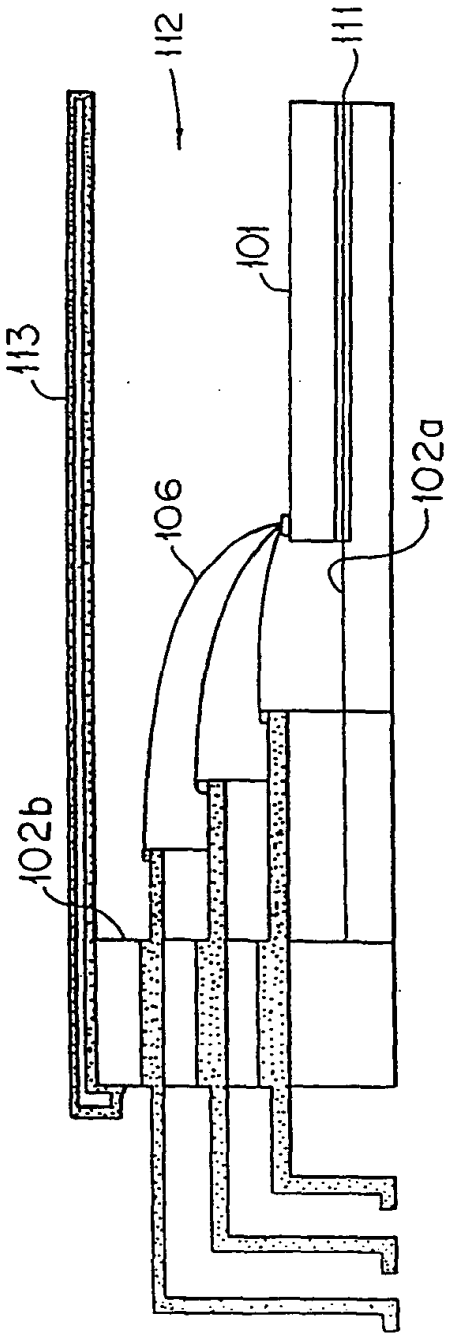

FIG. 4

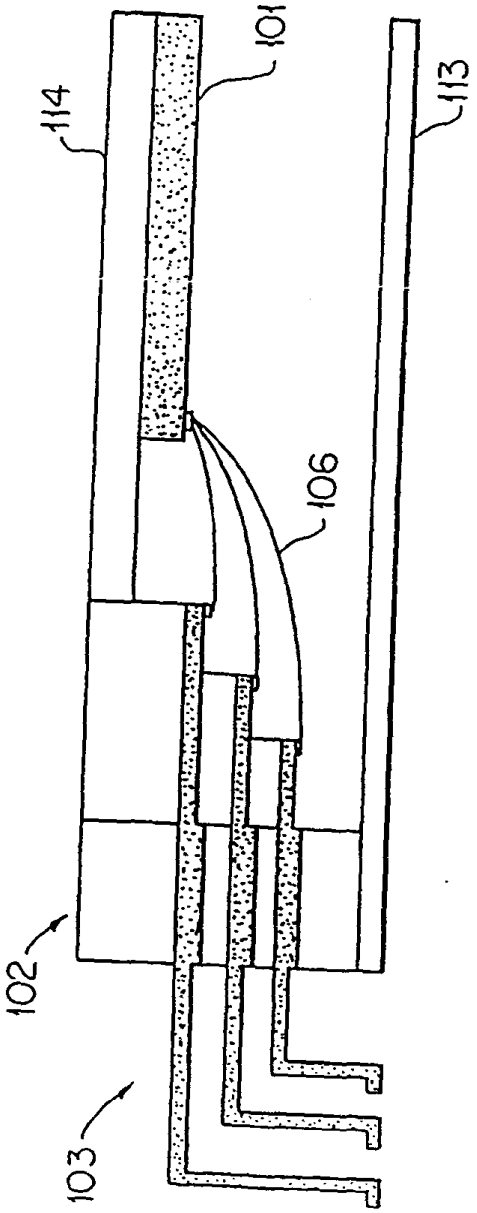

FIG. 5

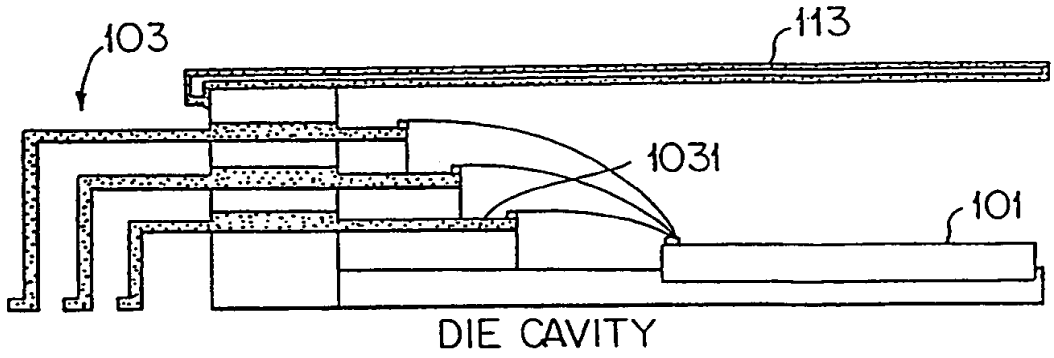

FIG. 6

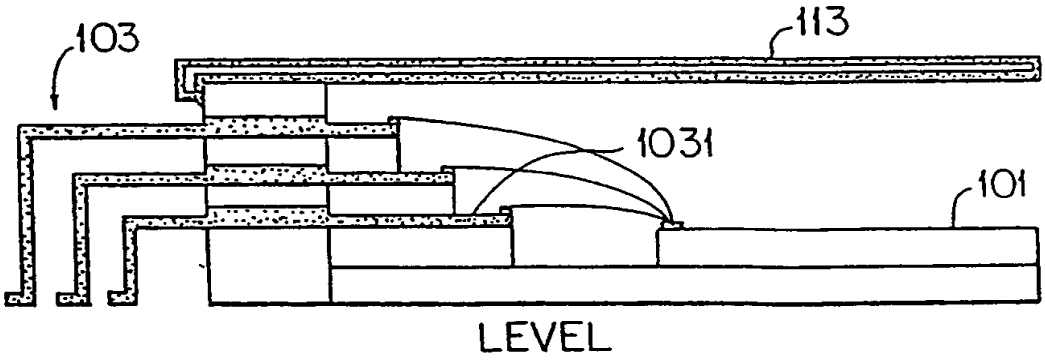

FIG. 7

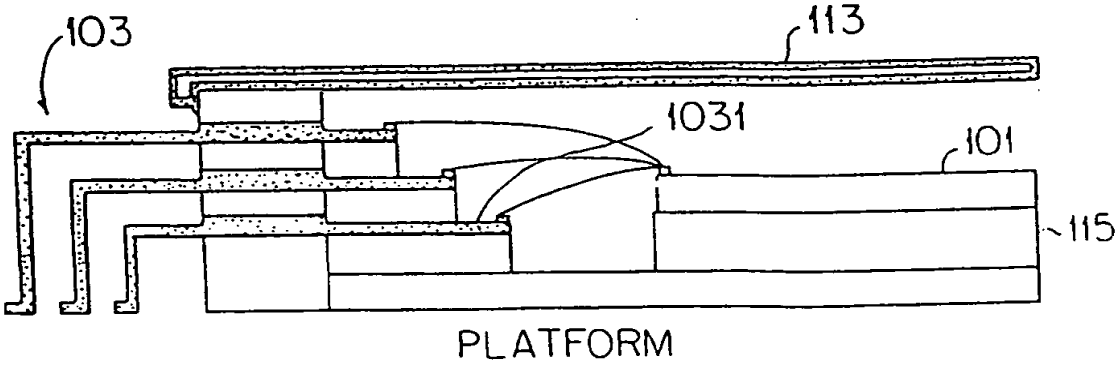

FIG. 8

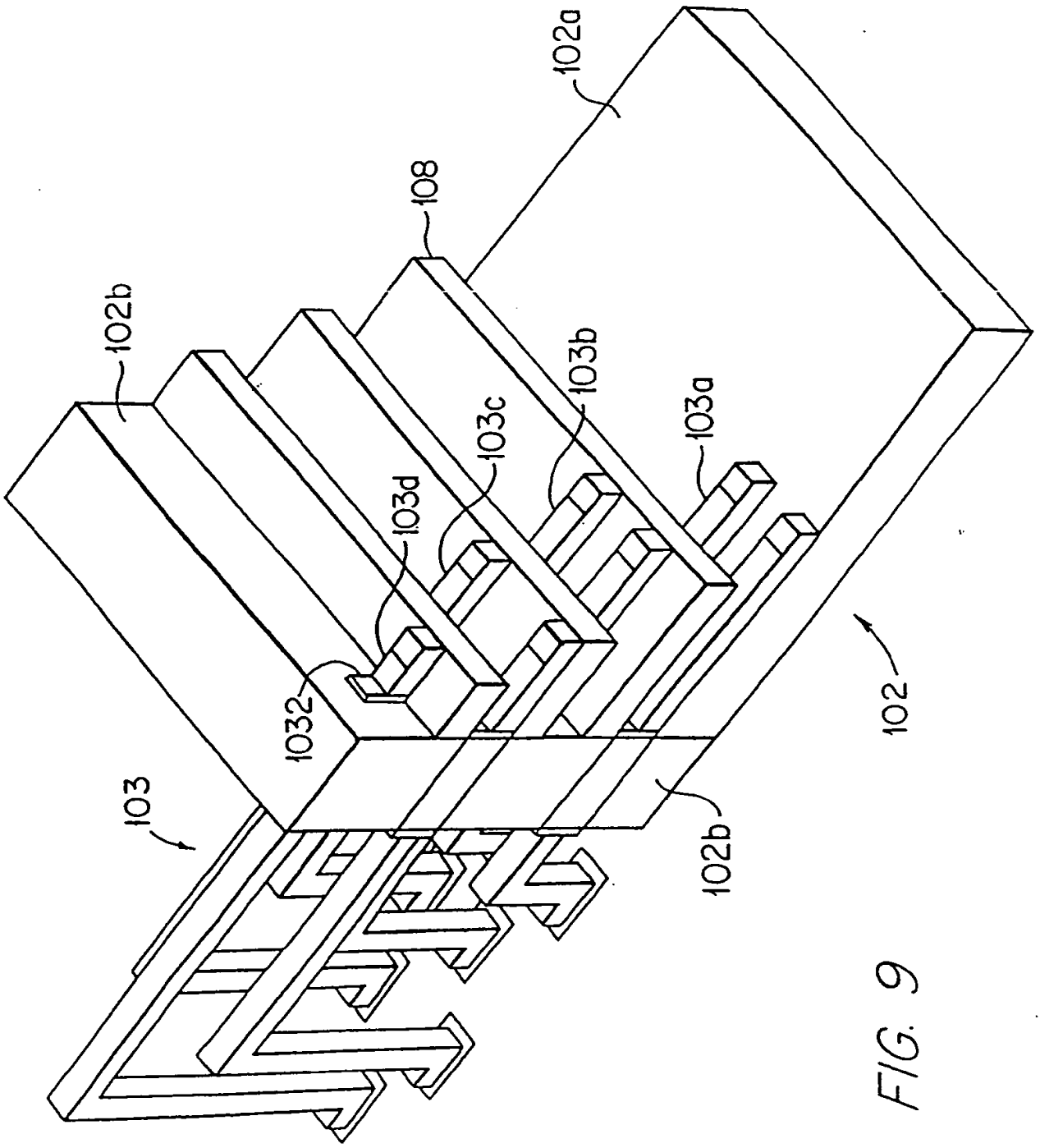

FIG. 9

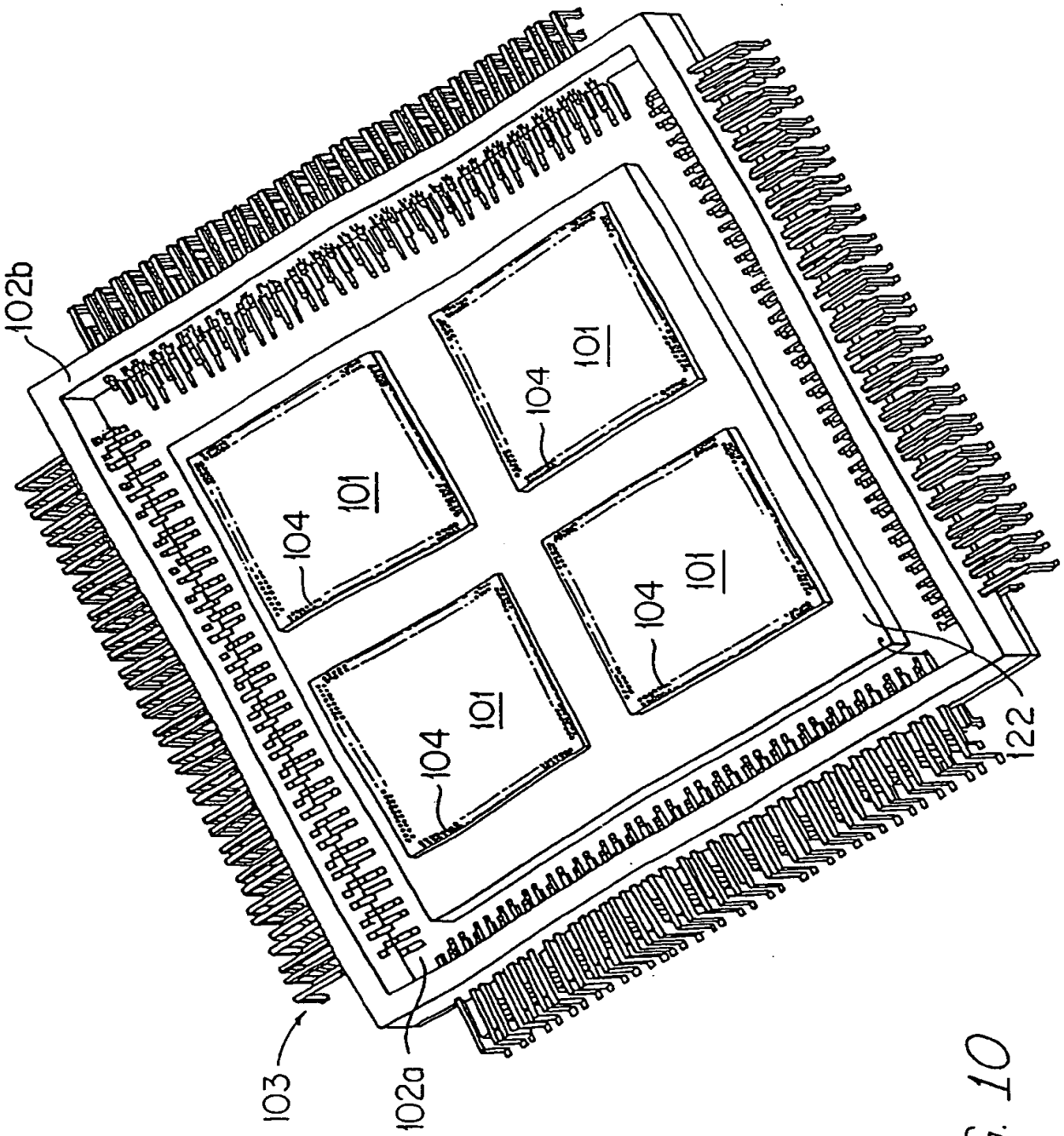

FIG. 10

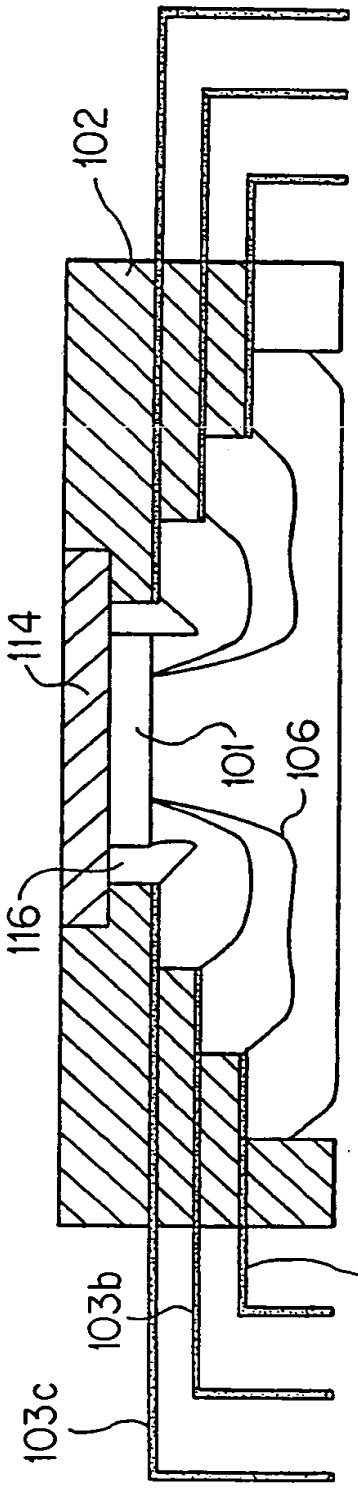

FIG. 11

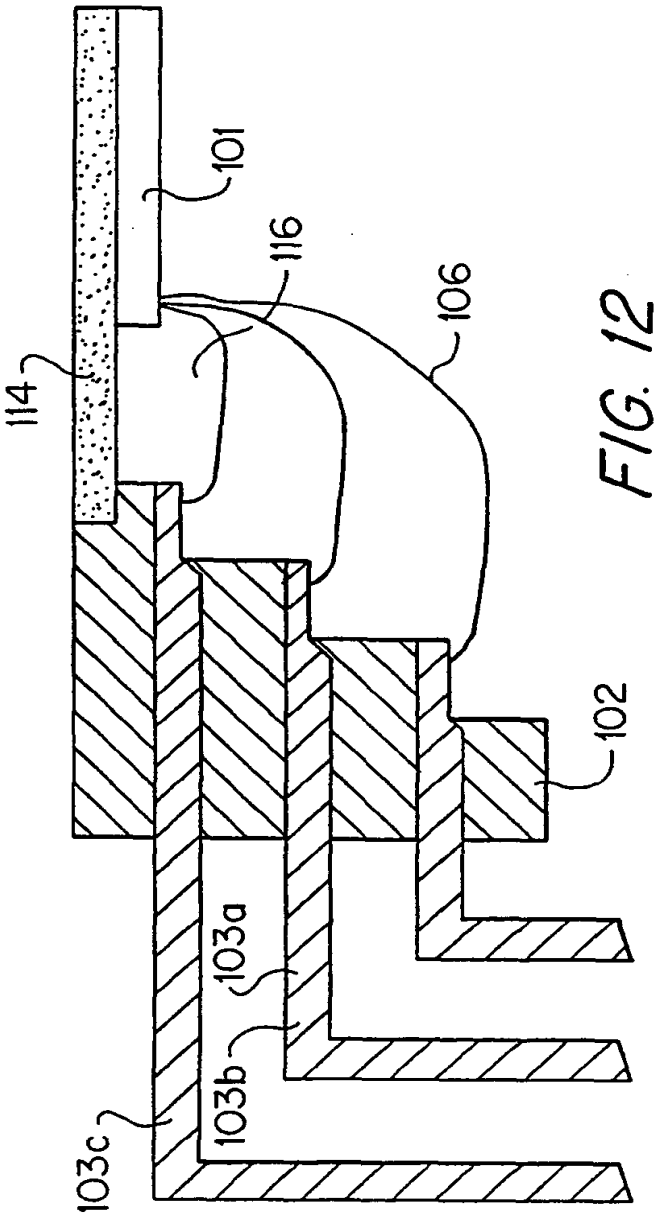

FIG. 12

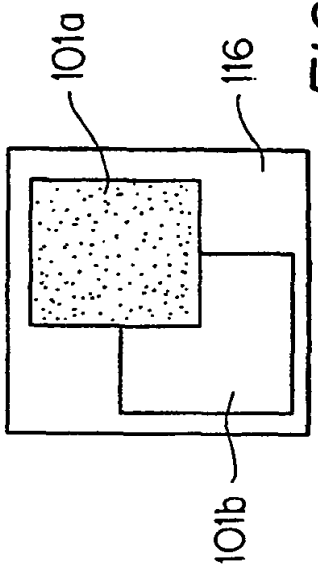

FIG. 13

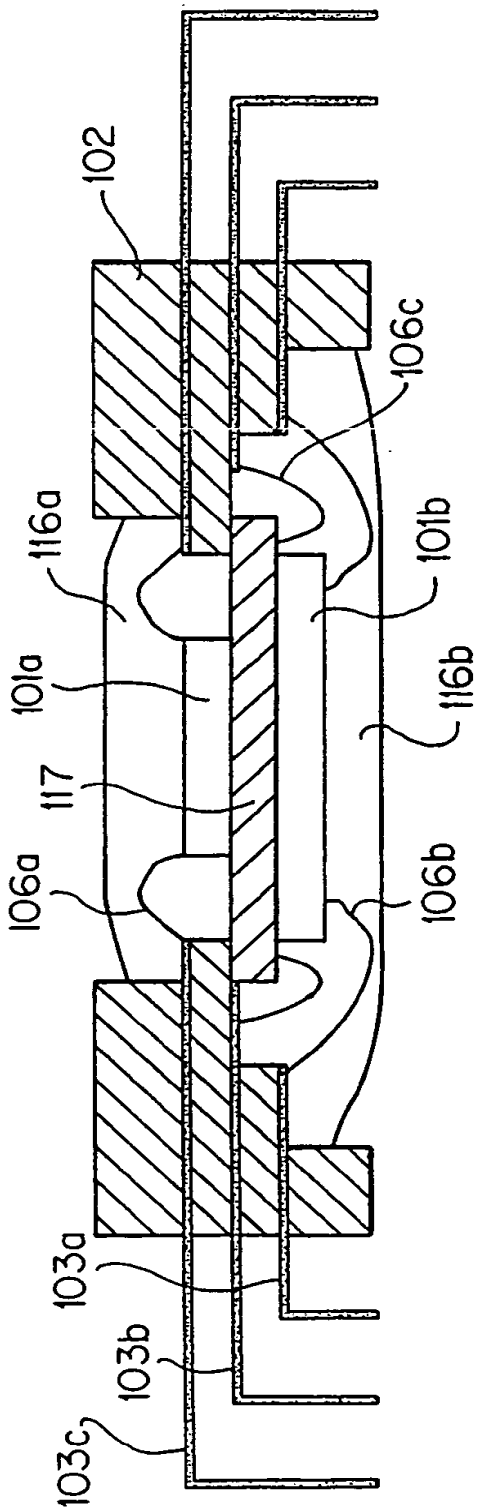

FIG. 14

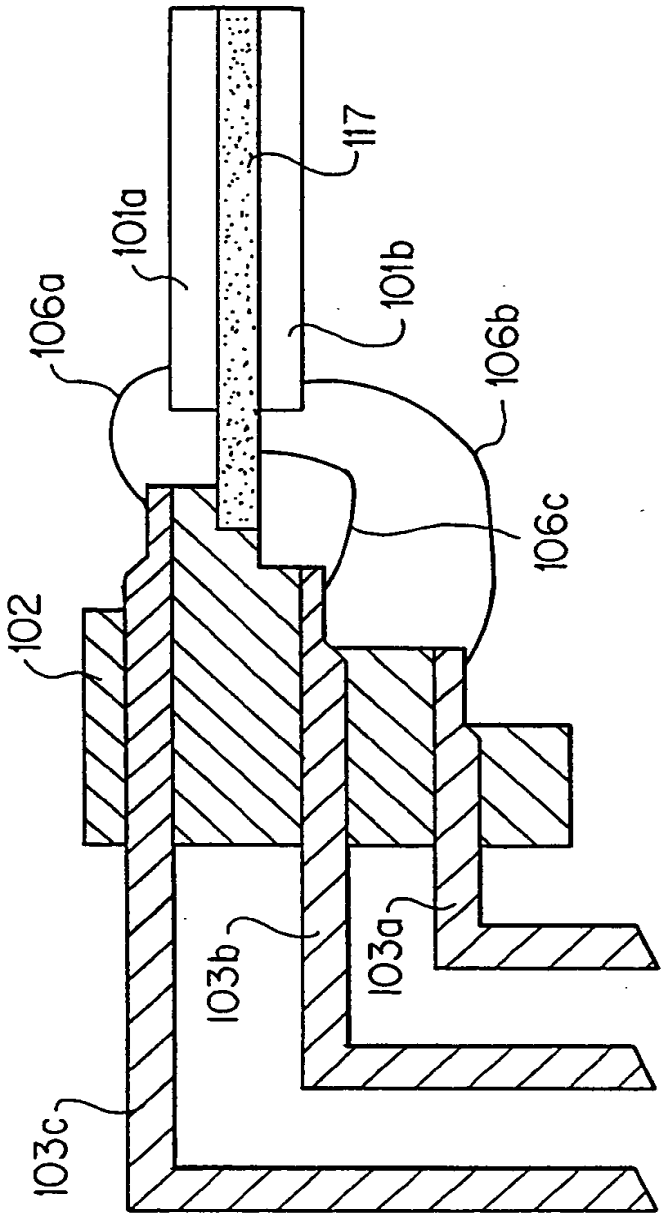

FIG. 15

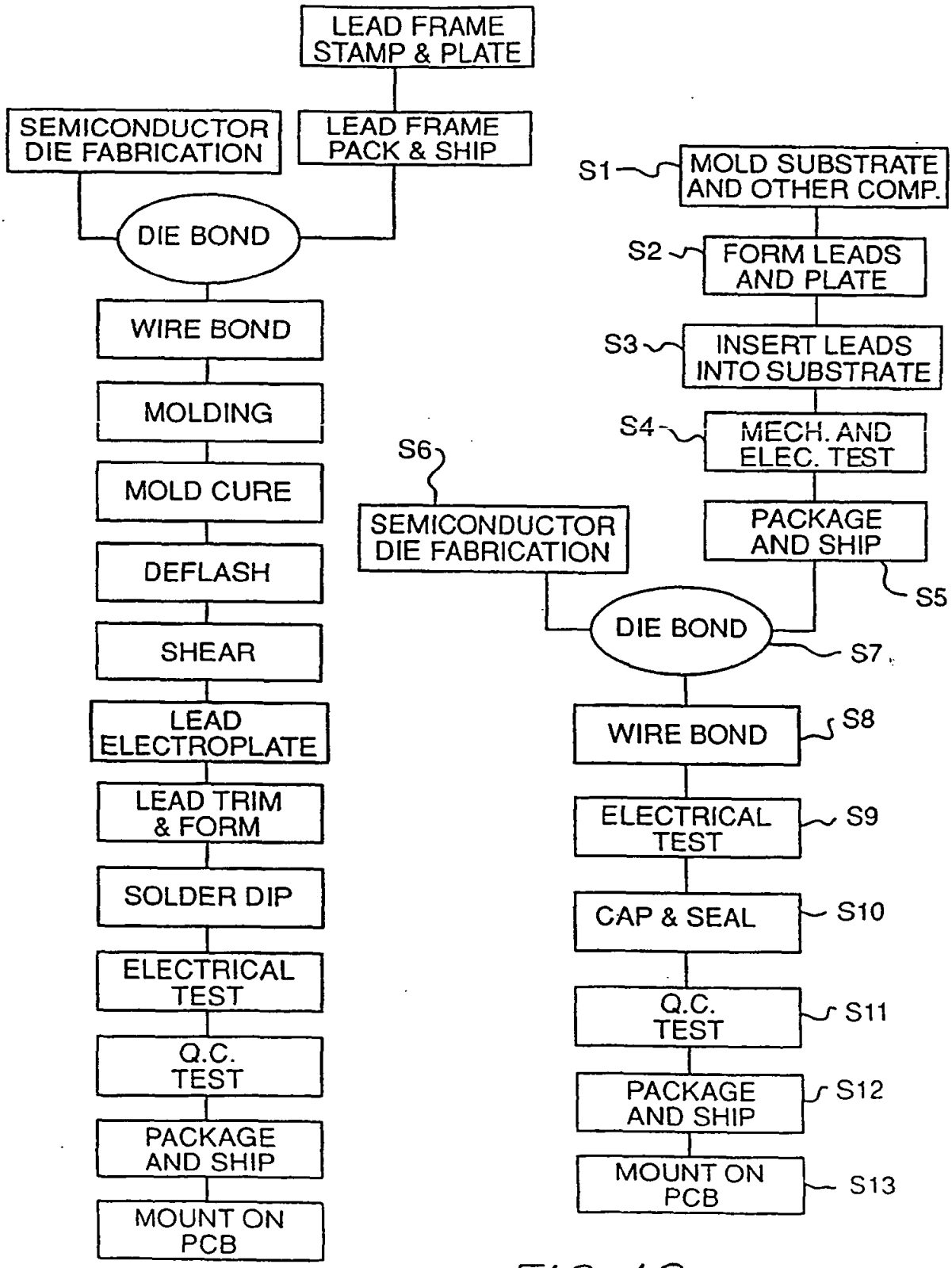

FIG. 16

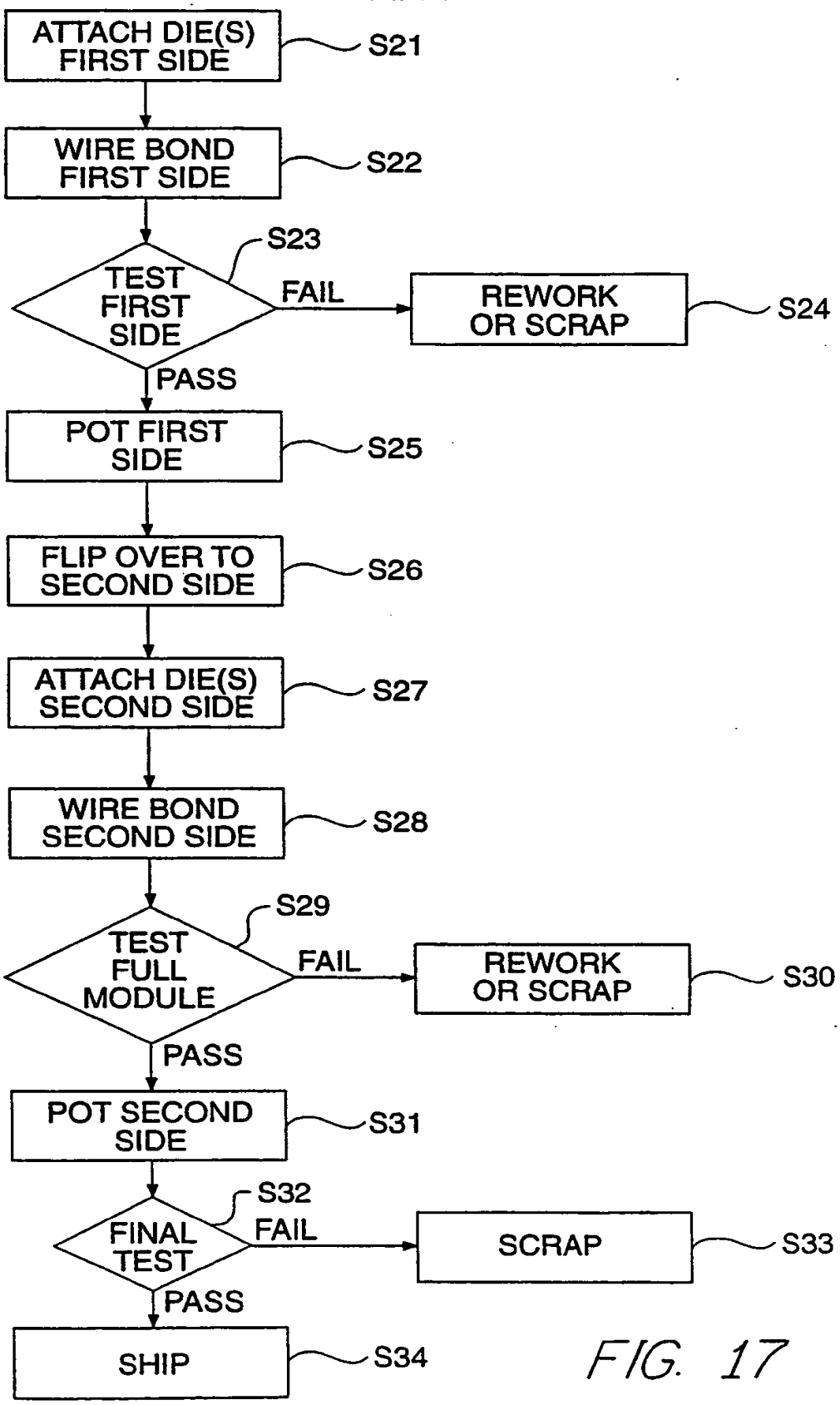

FIG. 17

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 96/09325

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L25/065

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 167 647 (SALERA) 11 September 1979 see the whole document ---	1,2,4,5, 7,10,11
X	US,A,5 220 491 (SUGANO ET AL.) 15 June 1993 see column 8, line 45 - line 65; figures 4,8,10,13,14 ---	1-5,11
X	US,A,4 423 468 (GATTO ET AL.) 27 December 1983 see figures ---	1-5,11
X	PATENT ABSTRACTS OF JAPAN vol. 7, no. 158 (E-186) & JP,A,58 066344 (HITACHI), 20 April 1983, see abstract --- -/--	1,2,4-6, 10,11

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 August 1996	30. 08. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Prohaska, G

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INTERNATIONAL SEARCH REPORT

Inte mal Application No
PCT/US 96/09325

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 12, no. 118 (E-600), 13 April 1988 & JP,A,62 248243 (MATSUSHITA), 29 October 1987, see abstract	1,2,4-6, 10,11
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 147 (E-323), 21 June 1985 & JP,A,60 028256 (FUJITSU) see abstract	6
A	US,A,5 327 325 (NICEWARNER, JR.) 5 July 1994 see the whole document	1-14

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

information on patent family members

Inte nal Application No
PCT/US 96/09325

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-4167647	11-09-79	NONE	
US-A-5220491	15-06-93	JP-A- 3291869	24-12-91
US-A-4423468	27-12-83	NONE	
US-A-5327325	05-07-94	NONE	